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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/994,261	11/26/2001	Albert Man	1376.0100660	8626

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EXAMINER	
TON, DAVID	

ART UNIT	PAPER NUMBER
2133	2

DATE MAILED: 02/24/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No. 09/994,261	Applicant(s) MAN ET AL.	
	Examin r David Ton	Art Unit 2133	

-- The MAILING DATE of this communication appears on the cover she t with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☐ Responsive to communication(s) filed on _____.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-22* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☒ Claim(s) *17-22* is/are allowed.

6)☒ Claim(s) *1-16* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *25 November 2001* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

1. The title of the invention is not descriptive. A new title is required that is clearly indicative of the invention to which the claims are directed.

2. Claims 1-22 are presented for examination.

Claim Rejections - 35 USC ' 103

3. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

4. Claims 1, 6 and 10 are rejected under 35 U.S.C. § 103 (a) as being unpatentable over Hoang et al. (Hoang) patent no. 6,357,026, in view of Zasio et al. (Zasio) patent no. 4,504,783 and further in view of Buckley et al. (Buckley) patent no. 5,969,756.

5. As to claim 1, Hoang teaches the invention substantially as claimed, including a method of production testing a video device [ASIC 12 of Fig. 1] comprising the steps of:

testing the device using scan techniques, wherein testing the device includes:

providing a first test vector [first binary pattern, see claim 1] to the device;

clocking [shifting, see claim 1] the device to assert the first test vector to the device;

providing a second test vector [second binary pattern, see claim 1] to the device;

receiving results from the first vector concurrently [simultaneously, see claim 4] with the steps of providing the second test vector; and

comparing the results with expected results [see "evaluation" in step iv of claim 7).

However, Hoang does not explicitly teach mounting a device on a tester fixture and serially loading test vector, wherein the test fixture is coupled to a general-purpose computer.

Zasio teaches a tester fixture [see Fig. 3] coupled to a computer [computing means, see claim 1 and col. 3 lines 29-32] for testing VLSI chip which is mounting on the tester fixture [mounting means, see claim 1] and transferring test data serially [see alternate serial in and serial output of Fig. 4 and claim 7].

It would have been obvious to one of ordinary skill in the Data Processing art at the time of the invention was made to combine the teachings of Hoang and Zasio by testing Hoang's ASIC on Zasio's test system. This modification would have been obvious and a person having ordinary skill in the art would have been motivated to do so because it would use Zasio's test system for testing, diagnostic and evaluations Hoang's ASIC.

Hoang and Zasio do not teach the device is a video device.
Buckley teaches a test system for testing an electronic display device.

It would have been obvious to one of ordinary skill in the Data Processing art at the time of the invention was made to modify Hoang's test system to adapt a specific device such as a video device taught by Buckley [see electronic display 12 of Fig. 1]. This modification would have been obvious and a person having ordinary skill in the art would have been motivated to do so because it would enhance the application of Hoang and Zasio test system

6. As to claim 6, Buckley teaches the device is a video processing device.

7. As to claim 10, Hoang teaches a JTAG port for interfacing [see claim 6 (test access port) and col. 3 lines 1-4 (IEEE 1149.1 standard)].

8. Claim 7 is rejected under 35 U.S.C. § 103 (a) as being unpatentable over Hoang et al. (Hoang) patent no. 6,357,026, in view of Zasio et al. (Zasio) patent no. 4,504,783 and further in view of Buckley et al. (Buckley) patent no. 5,969,756 and Blasco Allue et al. (Blasco) patent no. 6,691,270.

9. As to claim 7, Hoang teaches concurrently testing a set of components [two ASICs 12 & 14 of Fig. 1].

Hoang, Zasio and Beckley do not teach providing multiple chains of test vector values to separate sets of components of the device.

Blasco teaches a scan chain selector which providing multiple chains of test vector values to separate circuit elements of an IC wherein each scan chain coupled to a different one of the circuit elements [see claim 1].

It would have been obvious to one of ordinary skill in the Data Processing art at the time of the invention was made to modify the test system taught by Hoang to include a scan chain selector as taught by Blasco. This modification would have been obvious and a person having ordinary skill in the art would have been motivated to do so because it would provide the efficiency of the testing procedure of Hoang test system [see Blasco's abstract].

10. Claims 2-5 and 8-9 are rejected under 35 U.S.C. § 103 (a) as being unpatentable over Hoang et al. (Hoang) patent no. 6,357,026, in view of Zasio et al. (Zasio) patent no.

4,504,783, further in view of Buckley et al. (Buckley) patent no. 5,969,756 and Yousuf et al. (Yousuf) patent no. 6,128,757.

11. As to claim 2, Hoang, Zasio and Buckley do not teach step of determining, after the step of comparing the results, if the device has passed.

Yousuf teaches a screening process for testing integrated circuit on automated test equipment during production test by executing test vector of a functional test program, comparing the results of the functional test program with expected test results to determine if the IC passes the functional test; and, if so, performing further tests [see claim 1 and flow chart of Fig. 3, element 306].

It would have been obvious to one of ordinary skill in the Data Processing art at the time of the invention was made to combine the teachings of Hoang, Zasio and Yousuf to determine if the scan-test has passed before running further tests by performing the screening process as taught by Yousuf. This modification would have been obvious and a person having ordinary skill in the art would have been motivated to do so because it would save test time (by eliminate bad IC during screening process).

12. As to claims 3 and 5, Yousuf teaches isolating the good device and the bad device [element 306 of Flow chart of Fig. 3].

13. As to claim 4, Hoang teaches at-speed test [col. 1 lines 38-39].

14. As to claim 8, Hoang, Zasio, Buckley and Yousuf do not teach selecting one of an at speed test and a scan test mode and performing the test according to the selected test mode.

Official Notice is taken that selecting a test mode and performing the test according to the selected test mode is well known in the art.

It would have been obvious to one of ordinary skill in the Data Processing art at the time of the invention was made to modify the teachings of Hoang, Zasio, Buckley and Yousuf to include a test mode selection. This modification would have been obvious and a person having ordinary skill in the art would have been motivated to do so because it would provide the efficiency of the testing procedure of Hoang test system.

15. As in claim 9, Yousuf teaches orderly performing the test [see claim 1].

16. Claims 11-16 are rejected under 35 U.S.C. § 103 (a) as being unpatentable over Blasco Allue et al. (Blasco) patent no. 6,691,270 in view of St. Pierre, Jr. et al. (Pierre) patent no. 6,539,510.

17. As to claim 11, Blasco teaches the invention substantially as claimed, including a system [see Fig. 1] comprising:

A general purpose computer [PC 100 of Fig. 1] having a data processor [inherently], memory [inherently] and a communication port[parallel port of Fig. 1].

A test fixture [integrated circuit 120 of Fig. 1] having a communication interface [TAP of Fig. 1], a scan chain selector [Fig. 2], a control module [TAP controller 18 of Fig. 1].

Blasco do not teach a device socket for interfacing with a device.

Pierre teaches a system for implementing a boundary scan chain comprising an interface board having a socket for interfacing with an integrated circuit [see 5A and claims 1-2].

It would have been obvious to one of ordinary skill in the Data Processing art at the time of the invention was made to combine the teachings of Blasco and Pierre to provide a test system having a test fixture including a socket for interfacing with a device under test. This modification would have been obvious and a person having ordinary skill in the art would have been motivated to do so because it would provide an interface for selecting scan chains of the inserted device under test.

18. As to claims 12-13, Blasco teaches the port includes a JTAG port [see Fig. 1].

19. As to claims 14-15, Blasco teaches the scan chain is configured by a user to select said particular scan chain [col. 1 lines 54-68].

20. As to claim 16, Blasco teaches the device includes a graphics processor [processor core 140 of Fig. 1].

Allowable Subject Matter

21. Claims 17-22 are allowed.

Conclusion

22. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

23. Any inquiry concerning this communication or earlier communications from the examiner should be directed to David Ton, whose telephone number is (703) 306-3043. The examiner can normally be reached Monday through Thursday from 6:30 AM to 4:00 PM and alternate Friday from 6:30 AM to 3:00 PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Albert DeCady, can be reached at (703) 305-9595.

Any inquiry of a general nature of relating to the status of this application should be directed to the Group receptionist whose telephone number is (703) 305-9600.

Any response to this action should be mailed to:

Commissioner of Patents and Trademarks

Washington, D.C. 20231

or faxed to: (703) 872-9306

Hand-delivered responses should be brought to Crystal Park II, 2121 Crystal Drive, Arlington. VA., Sixth Floor (Receptionist).

DT

February 18, 2004

DAVID TON
PRIMARY EXAMINER